WHAT IS CLAIMED IS:

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      1. A delay time adjusting circuit which adjusts a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, the circuit comprising:

      first dividing means for dividing a frequency of said input signal by a first frequency division rate;

      delaying means for delaying said input signal by a predetermined time;

      second dividing means for dividing a frequency of said input signal delayed by said delaying means by a second frequency division rate;

      comparing means for comparing a phase of a signal generated by said first dividing means and a phase of a signal generated by said second dividing means; and

      adjusting means for adjusting said predetermined time according to a comparison result obtained by said comparing means.

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      2. The delay time adjusting circuit as claimed in claim 1, wherein said first frequency division rate is 1.

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      3. The delay time adjusting circuit as claimed in claim 1, wherein said comparing means

supplies a signal indicating said comparison result to said adjusting means according to said signal generated by said second dividing means.

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4. A delay time adjusting method which adjusts a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, the method comprising:
a first step of comparing a phase of a signal generated by dividing, by a first frequency division rate, a frequency of said input signal, and a phase of a signal generated by dividing, by a second frequency division rate, a frequency of said input signal delayed by a predetermined time; and
a second step of adjusting said predetermined time according to a comparison result obtained by said first step of comparing so that said phase of said signal generated by dividing by said first frequency division rate and said phase of said signal generated by dividing by said second frequency division rate match each other.

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5. The delay time adjusting method as claimed in claim 4, wherein said first frequency division rate is 1.

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6. The delay time adjusting method as claimed in claim 4, wherein said second step

includes adjusting said predetermined time at a
frequency according to said signal generated by
dividing by said second frequency division rate.